



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,998	11/26/2003	Daniel Mulligan	SIG000111	6604
34399 7590 03/31/2008 GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727				
EXAMINER				
BRADLEY, MATTHEW A				
ART UNIT		PAPER NUMBER		
2187				
MAIL DATE		DELIVERY MODE		
03/31/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/722,998

Applicant(s)

MULLIGAN, DANIEL

Examiner

MATTHEW BRADLEY

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SE/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 28 December 2007. Applicant's arguments have been carefully and fully considered but they are not persuasive. Accordingly, this action has been made FINAL.

The Examiner wishes to note that the reply filed on 28 December 2007 is not fully responsive to the prior Office Action because of the following omission(s) or matter(s): Applicant appears to have not responded to the Examiner's response to Applicant's arguments set forth in the Office Action mailed 2 May 2007 in that at least insofar as it appears to be clear, Applicant has repeated the previous arguments set forth in the "Remarks made in an amendment" of 8 February 2007. See 37 CFR 1.111.

Since the above-mentioned reply appears to be *bona fide*, and in view of compact prosecution, the Examiner has responded to Applicant's arguments by further clarifying the Examiner's position in the claim rejections and response to arguments *infra*.

Claim Status

Claims 1-20 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-20** are rejected under 35 U.S.C. 102 (e) as being anticipated by

Chrisop et al (U.S. Patent Application Publication 2003/ 0043638), hereinafter referred to as Chrisop.

As per independent claim **1**, Chrisop teach,

- determining mode of operation of the multiple function integrated circuit;
(Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identifying at least one active module of a plurality of modules of the multiple function integrated circuit requiring a buffer based on the mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate.*
- determining buffer requirements for the at least one active module; and
(Paragraph 0029)
- allocating memory space of the shared memory within the multiple function integrated circuit for the buffer to be used by the at least one active module (Paragraph 0025)

- wherein the plurality of modules of the multiple function integrated circuit and shared memory within the multiple function integrated circuit are both within a single integrated circuit (Paragraph 0023 and Paragraph 0031 – taught either as the RAM of itself or the allocator with the memory 120 as shown in Figure 1).

As per dependent claim 2, Chrisop teach, wherein the at least one active module comprises at least two of: a processing unit; universal serial bus (USB) device; digital to analog converter (DAC); and analog to digital converter (ADC) (Paragraph 0029). *The Examiner notes that, for example, the fax machine can be the device selected as the active module. This being the case, the fax machine contains a processing unit inside of it in addition to both a digital to analog converter that converts documents before sending over an analog communication medium as well as an analog to digital converter that converts incoming analog transmissions to digital documents. The same applies for a scanner and or a copier but the DAC and ADC have different inputs and outputs and outputs.*

As per dependent claim 3, Chrisop teach, wherein the mode of operation comprises at least one mode of operation selected from the group comprising: a digital audio player mode; a file storage device mode; a digital multimedia player mode; an extended memory device mode; a digital audio recorder mode; a digital multimedia recorder mode; and a personal data assistant (Paragraph 0023). *The Examiner notes that as taught by Chrisop, the “RAM is allocated to the temporary storage of documents.” Accordingly the system of Chrisop is acting as a file storage device.*

As per dependent claim 4, Chrisop teach,

- changing the mode of operation of the multiple function integrated circuit to a second mode of operation; (Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identifying at least one other active module of the plurality of modules requiring another buffer based on the second mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate. As taught in Paragraph 0029 of Chrisop, the system is able to allocate multiple areas of the RAM to different functions of the system.*
- determining buffer requirements for the at least one other active module; and (Paragraph 0029)
- allocating memory space of the shared memory for the another buffer to be used by the at least one active module (Paragraph 0025).

As per dependent claim 5, Chrisop teach, wherein the at least one active module has digital memory access (DMA) to the shared memory (Paragraph 0023). *The Examiner notes that the MFP system of Christop has access to digital RAM.*

As per dependent claim 6, Chrisop teach, wherein the shared memory comprises on-chip random access memory (Paragraph 0029). *The Examiner notes that the RAM is shown as on-chip RAM in figure 1 item 106.*

As per independent claim 7, Chrisop teach,

- determining a first mode of operation of the multiple function integrated circuit; (Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identifying at least one active module of a plurality of modules of the multiple function integrated circuit requiring a buffer based on the first mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate.*
- determining buffer requirements for the at least one active module; and (Paragraph 0029)
- allocating memory space of the shared memory for a buffer to be used by the at least one active module (Paragraph 0025).

As per dependent claim 8, Chrisop teach, detecting activation of the multiple function integrated circuit; (Paragraph 0023).

As per dependent claim 9, Chrisop teach,

- detecting a change from the first mode of operation of the multiple function integrated circuit to a second mode of operation; (Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identifying at least one active module of the plurality of modules of the multiple function integrated circuit requiring a buffer based on the second mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate. As taught in Paragraph 0029 of Chrisop, the system is able to allocate multiple areas of the RAM to different functions of the system.*
- determining buffer requirements for the at least one active module; and (Paragraph 0029)
- allocating memory space of the shared memory for a buffer to be used by the at least one active module module (Paragraph 0025).

As per dependent claim **10**, Chrisop teach, wherein the at least one active module comprises: a processing unit; universal serial bus (USB) device; digital to analog converter (DAC); and analog to digital converter (ADC) (Paragraph 0029). *The Examiner notes that, for example, the fax machine can be the device selected as the active module. This being the case, the fax machine contains a processing unit inside*

of it in addition to both a digital to analog converter that converts documents before sending over an analog communication medium as well as an analog to digital converter that converts incoming analog transmissions to digital documents. The same applies for a scanner and or a copier but the DAC and ADC have different inputs and outputs.

As per dependent claim **11**, Chrisop teach, wherein the first mode of operation and second mode of operation comprise at least one mode of operation selected from: a digital audio player mode; a file storage device mode; a digital multimedia player mode; an extended memory device mode; a digital audio recorder mode; a digital multimedia recorder mode; and a personal data assistant (Paragraph 0023). *The Examiner notes that as taught by Chrisop, the "RAM is allocated to the temporary storage of documents." Accordingly the system of Chrisop is acting as a file storage device.*

As per dependent claim **12**, Chrisop teach, wherein the at least one active module has digital memory access (DMA) to the shared memory (Paragraph 0023). *The Examiner notes that the MFP system of Christop has access to digital RAM.*

As per dependent claim **13**, Chrisop teach, wherein the shared memory comprises on-chip random access memory (Paragraph 0029). *The Examiner notes that the RAM is shown as on-chip RAM in figure 1 item 106.*

As per independent claim **14**, Chrisop teach,

- processing module; and (Figure 1 - allocator)

- memory operably coupled to the processing module, wherein the memory and processing module are within a single multiple function integrated circuit, wherein at least portion of the memory functions as the shared memory and wherein the memory stores operational instructions that cause the processing module to: detect activation of the multiple function integrated circuit; (Figure 1 item 120)
- determine a first mode of operation of the multiple function integrated circuit; (Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identify the at least one active modules of the multiple function integrated circuit requiring a buffer based on the first mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate.*
- determine buffer requirements for the at least one identified active module; and (Paragraph 0029)
- allocate memory space within the RAM for a buffer to be used by the at least one active module. (Paragraph 0025).

As per dependent claim 15, Chrisop teach,

- detect a change from the first mode of operation of the multiple function integrated circuit to a second mode of operation; (Paragraph 0023) *The Examiner notes that the system allocates RAM in response to prompts that correspond to a selected operation within the system.*
- identify at least one active module of the plurality of modules of the multiple function integrated circuit requiring a buffer based on the second mode of operation; (Paragraph 0023) *The Examiner notes that as discussed supra, the system allocates memory for a specific device within the multifunction peripheral device. Accordingly, the system of Chrisop identifies an active module from the multifunction peripheral device that requires memory to operate. As taught in Paragraph 0029 of Chrisop, the system is able to allocate multiple areas of the RAM to different functions of the system.*
- determine buffer requirements for the at least one active module; and (Paragraph 0029)
- allocate memory space of the shared memory for a buffer to be used by the at least one active module (Paragraph 0025).

As per dependent claim **16**, Chrisop teach, wherein the at least one active module further comprises at least one of: universal serial bus (USB) device; a flash memory device; an electronically programmable read only memory (EPROM) device; a multi-wire device; a hard drive device; digital to analog converter (DAC); and analog to

digital converter (ADC) (Paragraph 0024). *The Examiner incorporates by reference herein the comments made supra with respect to claim 1 and the fax machine.*

As per dependent claim 17, Chrisop teach, wherein the first mode of operation and second mode of operation comprise at least one mode of operation selected from: a digital audio player mode; a file storage device mode; a digital multimedia player mode; an extended memory device mode; a digital audio recorder mode; a digital multimedia recorder mode; and a personal data assistant (Paragraph 0023). *The Examiner notes that as taught by Chrisop, the "RAM is allocated to the temporary storage of documents." Accordingly the system of Chrisop is acting as a file storage device.*

As per dependent claim 18, Chrisop teach, wherein the at least one active module has digital memory access (DMA) to the shared memory (Paragraph 0023). *The Examiner notes that the MFP system of Christop has access to digital RAM.*

As per dependent claim 19, Chrisop teach, wherein the processing module determines the first mode of operation from initialization inputs to the multiple function integrated circuit, wherein the initialization inputs identify active modules operable coupled to the multiple function integrated circuit (Paragraph 0023-0025). *The Examiner incorporates by reference herein the comments made supra with respect to claim 1.*

As per dependent claim 20, Chrisop teach, wherein the active modules include at least one of: universal serial bus (USB) device; a flash memory device; an electronically programmable read only memory (EPROM) device; a multi-wire device; a hard drive

device; digital to analog converter (DAC); and analog to digital converter (ADC) (Paragraph 0024). *The Examiner incorporates by reference herein the comments made supra with respect to claim 1 and the fax machine.*

Response to Arguments

Applicant's arguments filed 28 December 2007 have been carefully and fully considered but they are not persuasive.

With respect to applicant's argument located within the last paragraph of the 7th page of the remarks (numbered as page 13) which recites:

*"With respect to Chrisop, the applicant respectfully submits at paragraph [0023] fails to teach, as is asserted by the examiner, **the allocation of shared memory within a multiple function integrated circuit**. Rather, Chrisop teaches that random access memory, RAM, may be adaptively allocated in a multi-function peripheral device. The applicant respectfully submits that within these multi-function peripheral devices, **RAM is a separate integrated circuit from the processor**." (emphasis added)*

The Examiner respectfully disagrees. The instant argument directed to claim 1 is not commensurate in scope with the claim language as the claim language clearly defines a method where insofar as it appears to be clear, Applicant's arguments are directed to a structure. Further, the Examiner is unsure as to where the processor, as argued by Applicant, is located within the limitations of claim 1. *If it is Applicant's intent for a processor to be recited in claim 1, then it must be clearly stated.*

Within the same argument, Applicant argues that Chrisop does not teach allocation of shared memory. The Examiner respectfully disagrees and notes that in paragraph 0023 of Chrisop, Chrisop teach allocation of RAM 'shared memory' for the

MFP function that is currently selected. Thus, Chrisop teach allocation of shared memory.

Further even assuming *arguendo* that Applicant's claim 1 recites a processor, and that 'shared memory within the multiple function integrated circuit are both within a single integrated circuit', the Examiner wishes to then draw Applicant's attention to Figure 1 items 104 and 120 as described in paragraph 0031 that show an allocator, processor, and memory combined on a single chip.

With respect to applicant's argument located within the first full paragraph of the 8th page of the remarks (numbered as page 14) which recites:

"This RAM is a separate integrated circuit and at no point does Chrisop teach that the MFP functions are executed within a single integrated circuit."

The Examiner respectfully disagrees. The Examiner notes that Chrisop teach execution of multiple functions, ie print, scan.. as shown in figure 1, of a multiple function device. When taken in its entirety, MFP 108 as shown in Figure 1 is a single integrated circuit. Further the Examiner wishes to draw Applicant's attention to Figure 1 items 104 and 120 as described in paragraph 0031 that show an allocator, processor, and memory combined on a single chip. Thus, Chrisop teach MFP functions being executed within a single integrated circuit.

With respect to applicant's argument located within the third and fourth full paragraphs of the 8th page of the remarks (numbered as page 14) as well as the argument located within the first full paragraph of the 12th page of the remarks (numbered as page 18) which recite arguments previously presented, the Examiner

respectfully disagrees and refers Applicants to the comments and rejections made *supra*.

Additionally, the Examiner notes the argument located within the first full paragraph of the 12th page of the remarks (numbered as page 18) which recites:

"The applicant respectfully submits that independent Claim 1 and independent Claim 14 have been amended to clearly restrict that the memory and processor to not be on a separate integrated circuits (i.e. a single IC chip)." (emphasis added)

The Examiner notes that there appears to be no amendments to claim 1 and no new amendments to claim 14 as stated in Applicant's argument noted above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Donald Sparks/
Supervisory Patent Examiner, Art
Unit 2187

DAS/mb